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Electrolyte-Gated, High Mobility Inorganic Oxide Transistors from Printed Metal Halides

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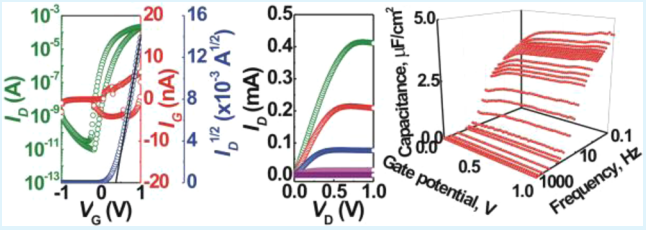
Supporting Information

ABSTRACT: Inkjet printed and low voltage (≤1 V) driven field-effect transistors (FETs) are prepared from precursor-made In_2O_3 as the transistor channel and a composite solid polymer electrolyte (CSPE) as the gate dielectric. Printed halide precursors are annealed at different temperatures (300–500 °C); however, the devices that are heated to 400 °C demonstrate the best electrical performance including field-effect mobility as high as 126 $cm^2\ V^{-1}\ s^{-1}$ and subthreshold slope (68 mV/dec) close to the theoretical limit. These outstanding device characteristics in combination with ease of fabrication, moderate annealing temperatures and low voltage operation comprise an attractive set of parameters for battery compatible and portable electronics.



KEYWORDS: *field-effect transistors (FETs), field-effect mobility, electrolyte-gating, oxide semiconductor, oxide electronics, solution-processed*

INTRODUCTION

Oxide semiconductor-based field-effect transistors (FETs) are attaining increasing research interest in solution-processed/printed electronics community because of their high intrinsic mobility, excellent environmental stability, high optical transparency, and ease of fabrication.[1−6] Exploiting these features (especially the outstanding electronic transport properties) oxide FETs are being considered for numerous novel applications including flexible displays, radio frequency identification (RFID) tags, electronic textiles,[7] photovoltaics,[8] smart sensors,[9] etc. In addition, electronic transport through oxide semiconductors is found to be quite insensitive to small chemical inhomogeneities or structural defects that make them quite attractive for low-cost solution processing/printing techniques.[10−14] Printing of functional oxide semiconductor layers is possible either from a stable nanoparticle dispersion (nanoink) or from a homogeneous solution of metal salts that preferentially decomposes at lower temperatures. The long-term stability of dispersions without excess polymeric stabilizers (which degrade electronic transport unless completely removed) limits particle loading in the nanoinks, resulting in highly porous films with reduced electrical performance, whereas metal precursors usually yield high-quality and structurally dense oxide layers. However, the unavoidable heating step associated with the precursor based synthesis technique in many cases limits the choice of inexpensive, flexible substrates.

In this report, we combine halide precursor based metal oxide (In_2O_3) active channels with electrolyte gating approach in order to assess the viability of low temperature treated and low voltage/power operated FET devices. Electrolyte gating simultaneously offers several advantages such as low drive voltage requirement,[14−16] easy device fabrication/printability and ability to follow nanosized corrugation of the active layer to form atomically smooth interface that enhances gating efficiency.[17] Although electrolyte-gated field-effect transistors (EG FETs) are often criticized for slow switching speed and limited environmental stability, however, in our previous publications we have demonstrated their thermal[18] and long-term environmental stability along with high switching speed.[14,19]

Indium oxide is a high band gap (3.7 eV) *n*-type semiconductor with high carrier concentration (>10^{18} cm^{-3})[20,21] and high intrinsic carrier mobility (~160 $cm^2\ V^{-1}\ s^{-1}$).[21] Consequently, In_2O_3 has been a favorite choice for researchers working with oxide FETs and numerous high performance devices have been prepared with ultrahigh vacuum

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(UHV) evaporated films (>120 cm^2 V^{-1} s^{-1}),[22] single-crystalline nanowires (~250 cm^2 V^{-1} s^{-1}),[23] or solution-based techniques (55 cm^2 V^{-1} s^{-1}, for devices that are annealed at 500 °C).[24] In this study, we demonstrate the superiority of the electrolyte gating approach which, because of its ultrasmooth interface formation and large polarizability, can lead to high electrical performance even for devices where the semiconducting channel still contains unremoved organic ligands as a result of low annealing temperatures. Additionally, this work also confirms the conclusion of our earlier publication (on room temperature processed FETs fabricated by printing indium oxide nanoparticle dispersions[17]) that the device mobility of the nanoparticulate channel FETs is completely determined by the large porosity and packing density of nanoparticles; ability to print a denser layer from a finely tuned nanoink or following a chemical sintering method can result in room-temperature-processed, high-performance oxide FETs.

EXPERIMENTAL SECTION

The precursor for indium oxide is prepared by dissolving 0.05 M $InCl_3.4H_2O$ in 1:1 ratio of deionized water and ethanol. The prepared sol is used as ink to print (using Dimatix 2831 inkjet printer) on the glass substrates with lithographically patterned passive (sputtered Sn-doped indium oxide, ITO) structures. The channel length (L) of the transistors is always defined by this lithography step and fixed to 50 μm, whereas the width ($W \approx 150$ μm) of the channel is determined by the size of the printed droplet which has varied a little from one device to the other. The printed structures are annealed in air at different temperatures (300−500 °C) for 1 h following a slow heating rate of 1 °C/min. The device fabrication is fairly straightforward where printing and annealing of such active channels has been followed by printing of a water based composite solid polymer electrolyte consisting of polyvinyl alcohol (PVA, Sigma-Aldrich, 98%), deionized water and potassium fluoride (KF, Sigma-Aldrich, 99.99%).[17] The detailed preparation of the FETs is presented in the Supporting Information; the transistors are built with the in-plane device geometry as have been reported earlier.[14,17]

RESULTS AND DISCUSSION

To characterize the indium oxide films, we also printed the prepared sol on separate reference glass substrates of the same batch which have then undergone similar annealing cycle as the devices and then are examined by X-ray diffraction, (XRD). The XRD patterns of annealed samples show (Figure 1a) highly crystalline phase-pure indium oxide for samples that are annealed at 400 and 500 °C (the corresponding In_2O_3 peaks are indexed according to ICSD No. 06−0416), however, for the samples that are heated to 300 °C, a secondary phase indium oxychloride (InOCl) is also observed (corresponding reflections are marked with * symbol), denoting incomplete hydrolysis/decomposition of the metal halide precursor. The calculated average crystallite size with respect to annealing temperatures are listed in Table S1 (Supporting Information). Generally, with other conditions remaining identical, the crystallite size tends to increase with the increase in annealing temperature; however, we observe larger average crystallite size for the 400 °C annealed samples compared to the ones annealed at 500 °C. The strain point[25,26] of the used float glass substrates being (490 °C) lower than the maximum annealing temperature may have led to certain surface roughness which in turn has promoted heterogeneous nucleation and has reduced the crystallite size.

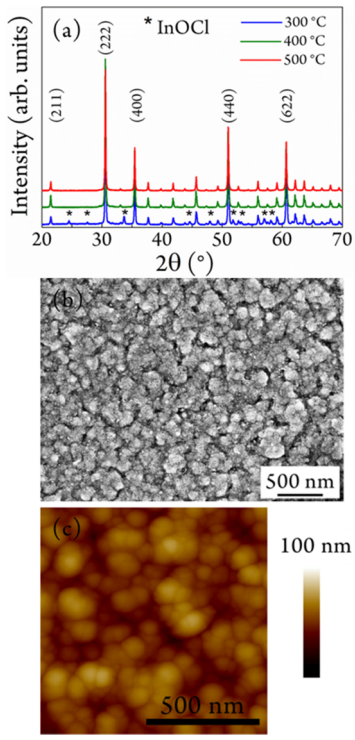

Figure 1. (a) XRD patterns of the precursors annealed at different temperatures (300−500 °C); (b, c) characteristic SEM and AFM micrograph of the printed precursor layer that has been annealed at 400 °C, respectively.

Scanning electron and atomic force micrographs (SEM & AFM) of transistor channels (printed droplets on passive structures) that are annealed at 300, 400, and 500 °C are shown in Figure S1 in the Supporting Information, images b and c in Figure 1b, and Figure S2 in the Supporting Information, respectively. Clearly, all the SEM images show solid network of particles and the observed particle match quite well with the avg. crystallite size obtained from the XRD data. The line profiles and the surface roughness analysis of the typical AFM micrographs (see Figures S3−S8 in the Suppporting Information) show a large surface roughness with the root-mean-square value of more than 5 nm in all cases. Such large roughness values in the present case can be an indication of the nonideal ink formulation in terms of the optimal fluid dynamic and ink-drying properties. In fact, it has previously been reported that when water is used as solvent (as in the present case) for metal halide precursors, the printed layers dry out very slowly and often result in a poor film quality.[5] Nevertheless, it may be noted at this point that in case of electrolyte-gated FETs surface morphology of the printed semiconductor layers is of limited importance, because the electrolyte can closely follow any sort of surface corrugation. It can be easily seen in the high resolution, cross-section SEM images shown in Figure 2 and Figure S9 in the Supporting Information. Thus a high-quality semiconductor-dielectric interface is usually guaranteed; this assumption is further confirmed by the outstanding electrical performance of our devices, described in the following paragraphs. Electrical characterization of the prepared EG FETs has been performed at room temperature in air. Relevant

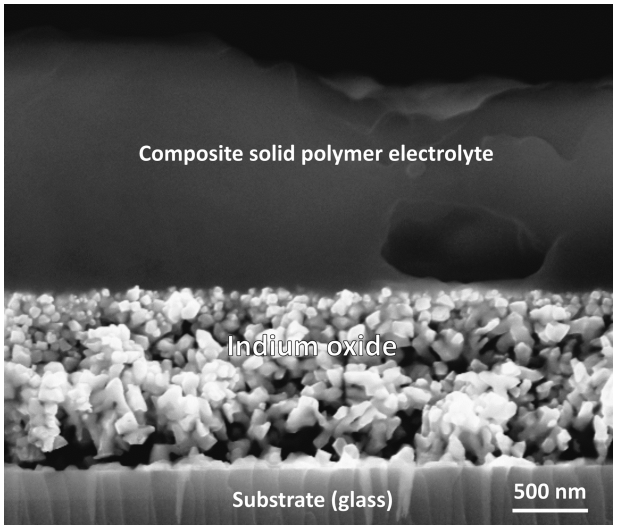

Figure 2. High-resolution cross-section SEM image of indium oxide semiconductor-CSPE dielectric interface, where the indium oxide precursor has been annealed at 400 °C.

transistor performance parameters of typical devices annealed at different temperatures are listed in Table 1.

Table 1. Complete Transistor Characteristics of Annealed Precursors at Different Temperatures (300−500 °C)

T (°C)	on/off ratio	$I_{D,sat}/W$ (μA/μm)	V_T (V)	S (mV/decade)	G_m (μS/μm)	μ_{FET} (cm^2/(V s))
300	3×10^5	0.8	0.15	126	2.7	23
400	2×10^7	2.4	0.37	68	3.3	126
500	3×10^5	2.4	0.16	126	5.5	63

All the devices show *n*-channel accumulation-mode MOSFET characteristics as expected for indium oxide. Interestingly, devices that are annealed at 300 °C also show reasonably high on-currents ($I_{D,sat}$= 0.8 μA/μm) and good device mobility (23 cm^2/(V s)), despite the presence of about 8% of an unwanted phase (see Figure S10 in the Supporting Information). However, the adverse effect of the spurious phase on electronic transport is evident in the drain current (I_D)−drain voltage (V_D) characteristic plot (Figure 3a) where a negative differential resistance (NDR)[27] effect is observed because of the charge traps caused by the leftovers of an insulating indium oxychloride. In contrast, the electrical performance of the FETs that are annealed at 400 °C is found to be quite outstanding and significantly better than the others (Figure 3b). A saturation drain current ($I_{D,sat}$) of 0.4 mA for a W/L ratio ~3 resulted in an excellent field-effect mobility value of 126 cm^2/(V s), whereas the subthreshold slope of the device calculated from the transfer curve has been only 68 mV/decade, very close to the room temperature theoretical limit of 60 mV/decade.[28] However, contradicting the general expectations, devices that are annealed at 500 °C do not show superior performance (Figure 3c) compared to the ones annealed lower temperature. The probable cause of this irregularity can be a slight softening of the substrate (silica glass) at 500 °C, which in turn results in a larger number of the crystallite nucleation sites; this is clearly reflected in the finer particles (see Figure S2 in the Supporting Information), lower avg. crystallite size (see Table S1 in the Supporting Information) and rough surface

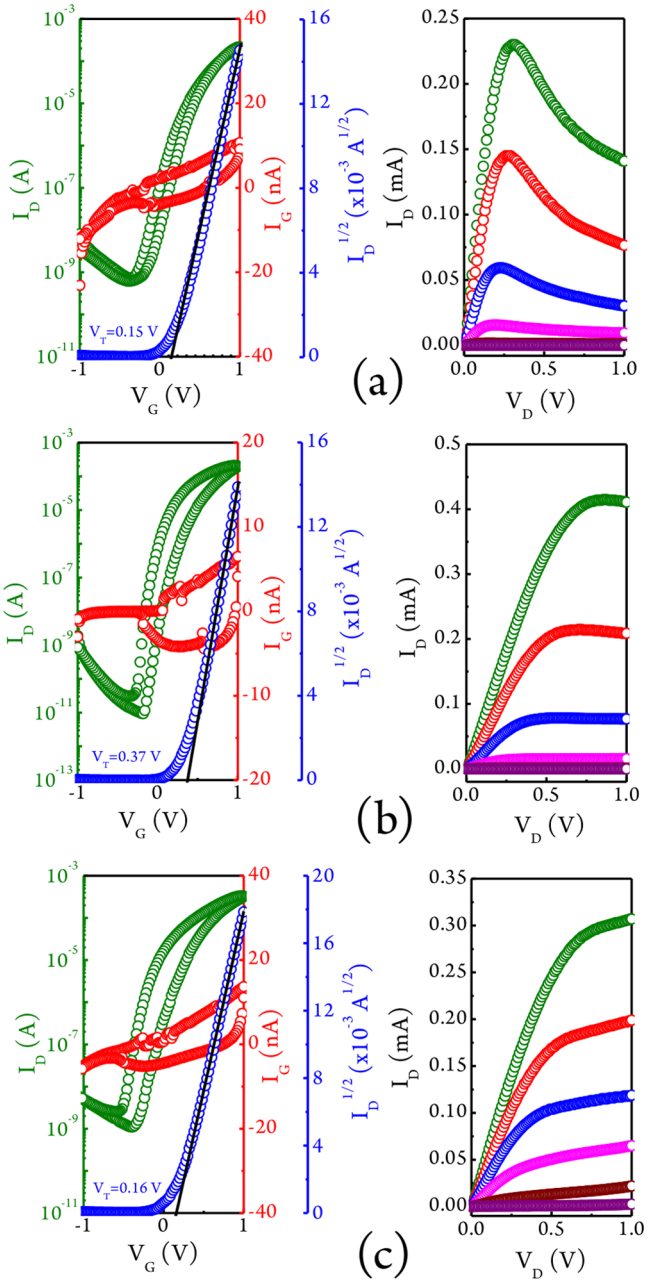

Figure 3. (a−c) Transfer characteristics and the drain current (I_D)−drain voltage (V_D) characteristics of typical transistor devices that are annealed at 300, 400 and 500 °C, respectively. In the transfer curves, green, red, and blue circles indicate the drain currents (I_D), the gate currents (I_G), and the square root of the drain currents ($I_D^{1/2}$) with linear fitting (black firm line), respectively. In the I_D−V_D measurements, the gate voltage (V_G) has been raised from 0 V (purple color circles) to 1 V (green color circles) with every 0.2 V increments.

(see Figures S7−S8 in the Supporting Information) in those films. All of these detrimental microstructural features have negatively affected the electrical performance; however, such high processing temperatures are anyway not acceptable for inexpensive and flexible polymeric substrates.

The performance figure of merit, field effect mobility (μ_{FET}) of the devices is calculated according to the following equation[29]

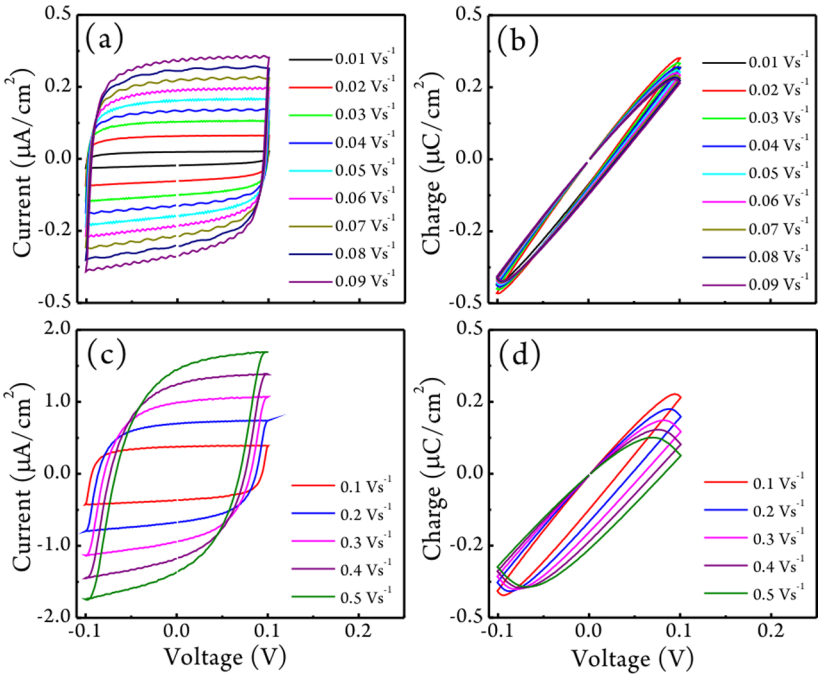

Figure 4. Cyclic voltammetry measurements with different scan rate. (a, c) Present current density and (b, d) accumulated charge vs voltage plots obtained for sputtered indium oxide thin films (with sputtered ITO as counter electrode). The scan rate variation of the constant current voltammetry sweeps are as follows: (a, b) 0.01−0.09 V s^{-1} and (c, d) 0.1−0.5 V s^{-1}.

$$I_{D,sat} = \frac{\mu_{FET} WC(V_G - V_T)^2}{2L} \quad (1)$$

where, $I_{D,sat}$, the saturated drain current; C, the specific capacitance at the transistor channel (in this case, $C = C_{dl}$; C_{dl}, the double layer capacitance); V_G and V_T, the gate and threshold voltage, respectively. Therefore, all other quantities being known, it is essential to estimate the double layer capacitance accurately in order to compute the device mobility values. However, in order to obtain accurate values experimentally, it is necessary to print continuous films over large enough area; unfortunately, such bigger printed areas always show considerable crack formation upon annealing. Hence, sputtered In_2O_3 films have been used to build parallel plate capacitors with a 50% larger (sputtered) ITO film as the counter electrode. This is believed to lead to a conservative estimation of field-effect mobility as the sputtered indium oxide films would essentially result in a larger double layer capacitance compared to the solution processed films. Cyclic voltammetry (CV) measurements for a ±0.1 V potential window, with 0.01−0.5 V/s scan rates are shown in Figure 4; the largest capacitance value is obtained to be of 3.75 $\mu F/cm^2$. It is also of practical interest to find out the capacitance at the highest gate potential that has been applied on devices (i.e., V_G = 1.0 V) in order to obtain saturated drain currents ($I_{D,sat}$); therefore, impedance measurements are performed to obtain differential capacitance at different dc bias voltage and at varied frequencies (Figure 5).

The capacitance values are calculated following the equation[14]

$$C_{eff} = -\frac{Z''}{\omega |Z|^2} \quad (2)$$

where C_{eff} is the gate voltage and frequency dependent capacitance, Z'' is the imaginary part of the total impedance; $|Z|$ is the impedance modulus, and ω is the angular frequency. What one can note from Figure 5 is that because of the large gap between the electrodes (2 mm), the capacitance value drastically drops from 0.1 to 1000 Hz (should not be the case for real devices for much shorter gate-channel distance); additionally, an insignificant change in capacitance values is noticed when sweeping the gate voltage from 0 to 1 V. This is because of the fact that the sputtered In_2O_3 films already possess large intrinsic carrier concentration without applied gate potential (hence they are also highly conducting); as a result, a large conductivity/capacitance modulation is not expected for the sputtered films, upon applied gate potential.[30] The situation for the solution processed films is clearly quite different as all of them show a very small channel (drain) current at the zero gate potential. Nevertheless, the high capacitance value of 4.33 $\mu F/cm^2$ obtained for 0.1 Hz at V_G = 1.0 V is taken as the double layer capacitance in order to

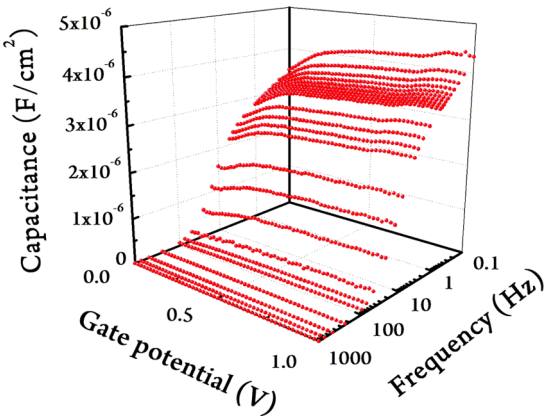

Figure 5. Measured effective capacitance on the sputtered In_2O_3 thin film with respect to ITO counter electrode, versus different applied gate potentials and varying frequencies (0.1−1000 Hz).

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calculate the device mobility. Moreover, the three-dimensional gating approach[17] of electrolytic insulator makes it necessary to consider the real surface area of the printed films instead of the projected ones. Therefore, this capacitance value is again corrected to take into account the nanosized corrugation of the printed channels and has been further raised by 10% for the 300 and 400 °C annealed films (see Figures S3–S6 in the Supporting Information) and even by 20% for the considerably rougher 500 °C annealed devices (see Figure S7–S8 in the Supporting Information). The calculated final μ_{FET} values are summarized in Table 1. Even after any possible overestimation in the C_{dl} calculations, the device annealed at 400 °C shows field-effect mobility value as high as 126 $cm^2/(V\ s)$; this not only signifies the potential and effectiveness of electrolyte gating in terms of excellent semiconductor-dielectric interface formation but also confirms high structural and electronic quality of the oxide channel, which is further evident from the good microstructural quality of the channels with the primary crystallite size larger than 100 nm. The environmentally friendly solvents that are used to prepare the printable sols/inks add to the merit of the whole device production process.

CONCLUSIONS

In summary, we have prepared indium oxide based FETs by inkjet printing using environment-friendly solvent based halide precursors. A composite solid polymer electrolyte has been used as an extremely efficient gate dielectric. The devices show a normally off accumulation-mode *n*-channel MOSFET operation with exceptionally high saturated drain currents and field-effect mobility values. Devices that are annealed at 400 °C (below the glass transition temperature of several low-cost commercial polymers) show over 120 $cm^2/(V\ s)$ field-effect mobility. The outstanding electrical performance together with the low voltage (drive voltages are always ≤1 V) and power requirements (off-currents of 1×10^{-10} to 1×10^{-11} A, has regularly been achieved) make them very much attractive for printable and portable electronics.

ASSOCIATED CONTENT

Supporting Information

The detailed preparation of field-effect transistors (FETs) and structural characterization of the printed In_2O_3 layers are presented. This material is available free of charge via the Internet at http://pubs.acs.org/.

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Notes

The authors declare no competing financial interest.

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